Post Doctorate Position
Cryogenic Analog Front-End for Quantum Computing

Location: Grenoble, France
Profile: PhD with significate background in microelectronics, especially integrated design
Funding: <2200€/month net
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Resume

Quantum engineering is a rapidly evolving novel domain in device technology, boosted by the recent progress in semiconductor quantum bits (QuBits) and by the major opportunity to combine the quantum device with dedicated electronics of conventional CMOS technology working at low temperatures (≤ 4 K). The ultimate goal of the research related to the proposed post PhD will be the development of silicon-based systems containing many QuBits and versatile electronics based on mature industrial technology, in order to facilitate the massive introduction of quantum processors. Nowadays state-of-the-art experiments on low-temperature quantum devices use electronic components at room temperature, but the future development of integrating many QuBits together complicates the device control with the multiplication of data lines. Minimal power dissipation and noise characteristics will be the challenging key elements to control a large number of QuBits. At CEA Grenoble, we have developed the first semiconductor QuBit fully realized on a CMOS 300-mm foundry that uses the spins of holes in Si as quantum state. The subject of the post PhD is aimed to build the electronics needed nearby the QuBit at low temperatures, using industrial CMOS technology (FDSOI 28nm) compatible with Silicon Qubits. The post PhD will be asked to develop his competence in the quantum physics of QuBits, the modelling of transistor parameters at low temperatures, and the design and measurement of analogue electronics, with the main task in developing and testing CMOS circuitry at low temperatures.

Detailed subject

Context

Large-scale quantum computers would theoretically be able to solve certain problems much more quickly than any classical computers that use even the best currently known algorithms. This computing supremacy would allow a quantum computer to decrypt many of the cryptographic systems in use today. Google has announced that it expects to achieve quantum supremacy soon, and IBM says that the best classical computers will be beaten on some task within about five years.

A variety of elementary qubits have already been proposed and experimentally demonstrated in academic research laboratories. CEA (Maurand, Nature Com'16) was recently shown that a spin in silicon can hold a bit of quantum information. This demonstration makes it an attractive and industrial credible option for the realization of a quantum computer. Recently, the implementation of Si spin qubit on a foundry-compatible CMOS SOI platform was demonstrated in CEA, marking an important first step towards the realization of a Si-based quantum computer using well-established industrial process: the CMOS. But, numerous qubits need to be individually addressed in a quantum processor i.e. initialized, manipulated, and measured. This large-scale parallelism seems hardly manageable without the use of co-integrated front-end electronics whish address dense qubits array. Therefore, analysis the operation of electronics to cryogenic temperatures (around 1K and below) appears as an urgent task to undertake in parallel with qubit development.

Post-doctoral work

The objective of this post-doctoral project includes the development of integrated circuits in 28nm FDSOI technology around 1 Kelvin to read the spin direction of on-die Silicon Quantum bits (Qubit). As the project has a multidisciplinary scope, the candidate has to create strong interfaces with the other labs in CEA Grenoble in charge of characterization and modeling of the transistors at low temperature and involved in Qubit definition. Thanks to the discussion with Physicists who have already a bulky test-bench to measure their Qubit, he/she has to define the best electronics topology and sensing operation to read the Qubit without erasing its state. At first order, the small gate capacitance variation due to a quantum effect has to be measured to have a picture of spin orientation. Based on a preliminary low-temperature design kit, the candidate has to define which analog block could be integrated in the same die than qubit around 1K. The limited power dissipation due to fridge capability, the bandwidth and noise level required to sense efficiently the spin state could not be achievable with electronics due to a lower performance at low temperature then these constraints will shape the design boundaries. The next step is to design at transistor-level, fabricate through MPW projects (using STMicroelectronics fab'), and characterize the defined analog front-end including some quantum elements to mimic the Qubit. A qubit arrays (>100) will also be studied to determine which analog front-end could be integrated inside a large qubit matrix in quantum processor context. The candidate will be helped by senior analog designers, other PhD students or post doc' involved in this project (~5). Some scientific exchanges with other international leader labs are also planned. The candidate will be involved in other experiments done by other research CEA groups around cryoelectronics topics. His/her research will be published in high-impact factor: nowadays no analog front-end is integrated around the qubit and any proof of concept will have a high impact on the quantum community. This research topic is top-priority for CEA to allow a computing breakthrough by developing the first Silicon-based quantum computer.